high voltage pulse can be reduced, electric damage on the electric loads 21, 22 can also be controlled.

[Third Embodiment]

Fig. 14 shows a high voltage pulse detecting circuit 83 included in the voltage regulator 6 of the alternator 1 according to a third embodiment.

The high voltage pulse detecting circuit 83 comprises a high voltage pulse detecting section 160, a discriminating section 170 and an output control section 180. This high voltage pulse detecting circuit 83 is different from the high voltage pulse detecting circuit 83 of the second embodiment shown in Fig. 9.

The discriminating section 170 is provided with a timer 171, AND gates 172, 174, a pulse counting circuit 173 and a pulse duration measuring circuit 175. It further comprises a timer circuit 183 and an OR gate 184. The additional timer circuit 183 receives the input of the output signal of the pulse counting circuit 173, while the OR gate 184 receives input of each output signal of two timer circuits 181, 183. The output signal of the OR gate 183 is inputted as a reset pulse to the pulse duration measuring circuit 175 and pulse counting circuit 173. The pulse counting circuit 173 and pulse duration measuring circuit 175 correspond to the memory means, while the timer circuit 183, and the OR gate 184 correspond to the reset signal generating means, respectively.

Fig. 15 shows signal waveforms inputted or outputted to or from each section of the high voltage pulse detecting circuit

83 of this embodiment. Fig. 16 is a diagram for comparing the signal waveforms to be inputted or outputted to or from each section of the high voltage pulse detecting circuit 83 shown in Fig. 9.

When connection of an inductive load (for example, a motor to rotate an electric fan, or the like) is cut off with a relay or a switch or the like, chattering occurs depending on the response characteristic of the relay or the like. Even when the cut-off operation is performed once, it is probable that the high voltage pulses are generated several times.

In the high voltage pulse detecting circuit 83 shown in Fig. 9, if a high voltage pulse higher than the reference voltage V3 is generated several times as shown in Fig. 16, the voltage comparator 66 outputs the high level signal several times corresponding to such high voltage pulses. In synchronization with the rising edge of this signal, the timer circuit 171 starts the operation. The AND gate 172 passes the output signal of the voltage comparator 66, while the timer circuit 171 is in the operative condition. The pulse counting circuit 173 outputs the high level signal when the pulses are inputted two times or more and the AND gate 174 outputs the high level signal only for the pulse duration. The pulse duration measuring circuit 175 measures the pulse duration and holds the pulse. Thereafter, since the pulse counting circuit 173 maintains the high level output, the pulse duration is accumulated in the pulse duration measuring circuit 175 for each generation, whenever the high voltage pulse is generated due to the cut-off condition of load.

When the accumulated duration exceeds the predetermined accumulated period, the pulse duration measuring circuit 175 outputs the high level signal. With this high level signal, the timer circuit 181 operates, followed by operation of the output control circuit 182, to control the power generation output. Accordingly, the output voltage of the alternator 1 is lowered. Upon completion of operation of the timer circuit 181, the reset pulse is inputted to the pulse duration measuring circuit 175 and pulse counting circuit 173 to reset the data of accumulated period and pulse count number.

Next, operation to avoid such unnecessary power generation control will be explained with reference to Fig. 15.

In the high voltage pulse detecting circuit 83 shown in Fig. 14, the timer circuit 183 starts operation when an output of the pulse counting circuit 173 rises to the high level. This timer circuit 183 generates the reset pulse after the predetermined time has passed and the accumulated period data and pulse count number are reset earlier than output of the reset pulse from the timer circuit 181. Thereafter, a single high voltage pulse generated in a certain case because the cut-off condition of load is not accumulated and the output control circuit 182 does not operate.

Even in the case where there is no particular contact failure of the power supply line 8, if a high voltage pulse is generated due to the chattering phenomenon when the load is cut off depending on the response characteristic of a relay or the like to control the on/off conditions of the electric load 21,